COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4028B

PRELIMINARY DATA

BCD-TO-DECIMAL DECODER

- BCD-TO-DECIMAL DECODING OR BINARY-TO-OCTAL DECODING
- HIGH DECODED OUTPUT DRIVE CAPABILITY
- "POSITIVE LOGIC" INPUTS AND OUTPUTS: DECODED OUTPUTS GO HIGH ON SELECTION
- MEDIUM-SPEED OPERATION: t_{PHL}, t_{PLH} = 80 ns (TYP.) @ V_{DD} = 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4028B** (extended temperature range) and **HCF 4028B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4028B** types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

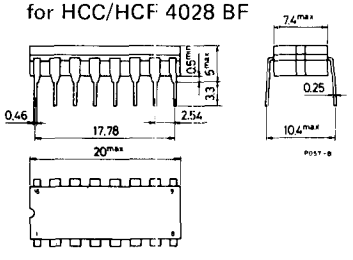
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

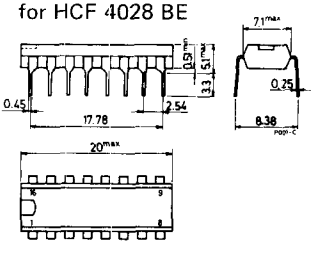
HCC 4028 BD for dual in-line ceramic package
HCC 4028 BF for dual in-line ceramic package, frit seal
HCC 4028 BK for ceramic flat package
HCF 4028 BE for dual in-line plastic package
HCF 4028 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

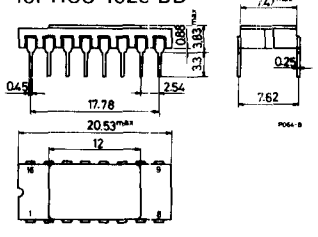
Dual in-line ceramic package
for HCC/HCF 4028 BF



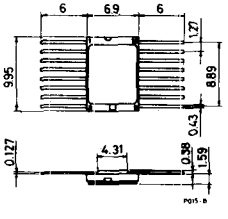
Dual in-line plastic package
for HCF 4028 BE



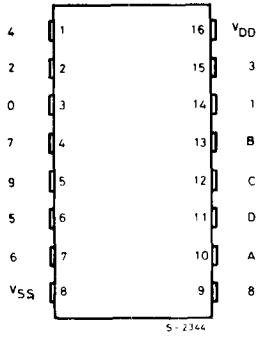
Dual in-line ceramic package
for HCC 4028 BD



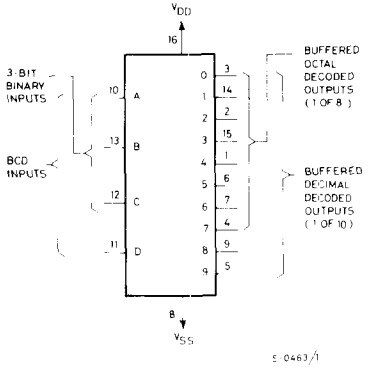
Ceramic flat package
for HCC 4028 BK



CONNECTION DIAGRAM



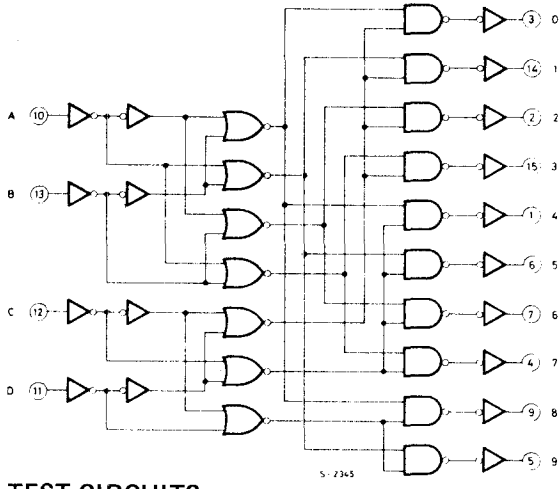
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

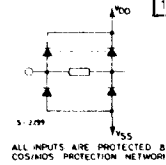
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM AND TRUTH TABLE



D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

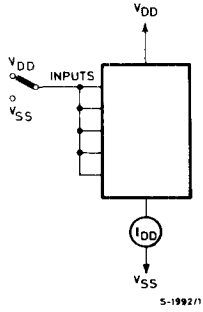
WHERE 1 = HIGH LEVEL
0 = LOW LEVEL



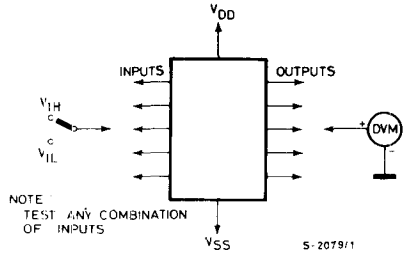
ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK.

TEST CIRCUITS

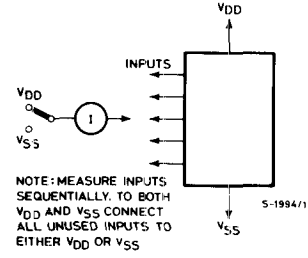
Quiescent device current



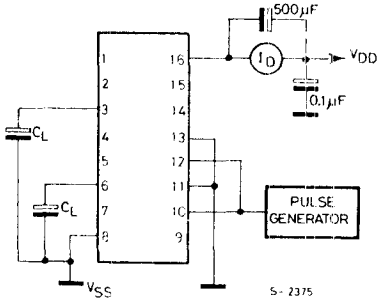
Noise immunity



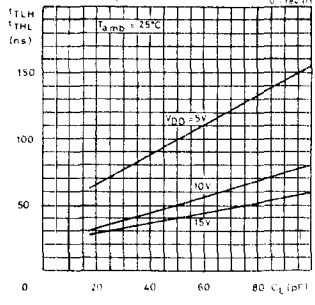
Input leakage current



Dynamic power dissipation



Typical transition time vs. load capacitance



STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		± 0.1		$± 10^{-5}$	± 0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

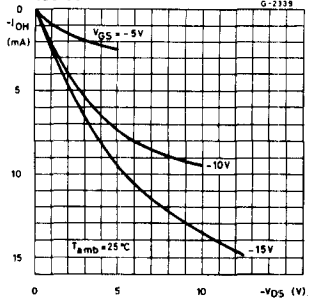
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

**Any input

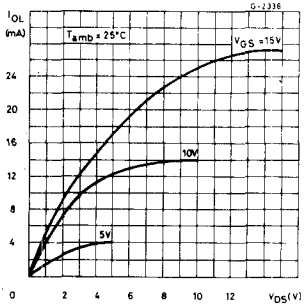
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD}(V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time (Clock to "Out")		5		175	350	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

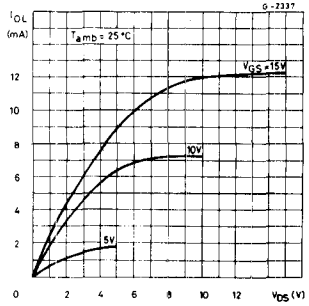
Minimum output high (source) current characteristics



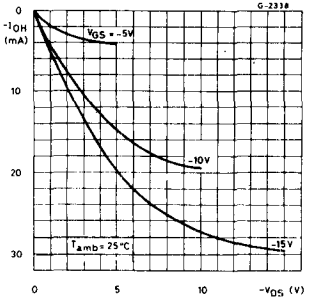
Typical output low (sink) current



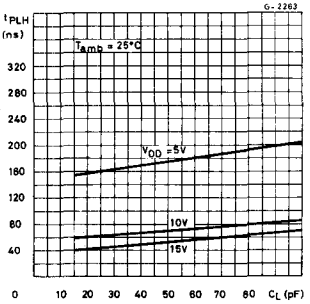
Minimum output low (sink) current characteristics



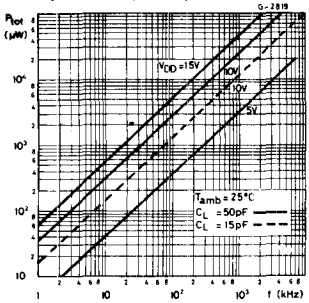
Typical output high (source) current characteristics



Typical propagation delay time as a function of load capacitance



Typical dynamic power dissipation as a function of input frequency



TYPICAL APPLICATIONS

The circuit shown in fig. 1 converts any 4-bit code to a decimal or hexadecimal code. Fig. 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input pins of the HCC/HCF 4028B to select a particular output. For example: in order to get a "high" on output n. 8 the input must be either an 8 expressed in 4-bit binary code, a 15 expressed in 4-bit Gray code, or a 5 expressed in Excess-3 code.

Fig. 1 - Code conversion circuit

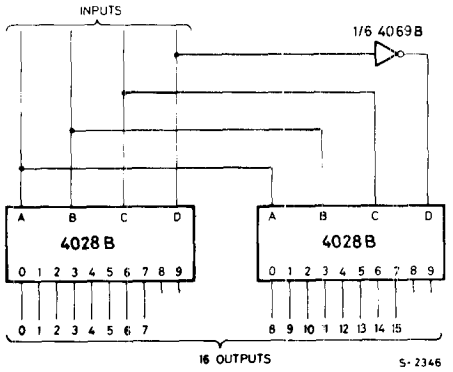


Fig. 2 - Code conversion chart

INPUTS				INPUT CODES				OUTPUT NUMBER																				
				Hexa Decimal	Decimal																							
D	C	B	A	4 BIT BINARY	4 BIT GRAY	EXCESS 3	EXCESS 3 GRAY	AIKEN 4221	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 4 - Neon readout (Nixie Tube) display application

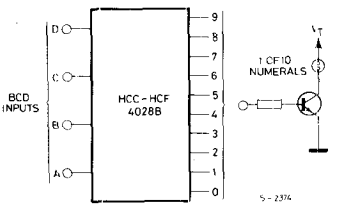


Fig. 3 - 6-bit binary to 1 of 64 address decoder